forming a number of gate lines on the gate insulator layer; and

forming a number of anodes opposite the emitter tips;

wherein a distance separating the number of cathode emitter tips from the number of gates lines is significantly thinner than a separation distance separating the number of gate lines and the substrate[.] ;

a row decoder and a column decoder each coupled to the field emitter array in order to selectively access the pixels; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

47. (Amended) A field emitter array, comprising:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes.

51. (Amended) A field emitter array, comprising:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes;

wherein the number of cathodes include metal silicides on the polysilicon cones.

52. (Amended) A field emitter array, comprising:

a number of cathodes in rows along a semiconductor-on-glass substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness; and

a number of anodes located in columns orthogonal to and opposing the rows of cathodes.

53. (Amended) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially thinner than the gate line region thickness;

a number of anodes located in columns orthogonal to and opposing the rows of cathodes; and

a row decoder and a column decoder each coupled to the field emitter array; and

a processor adapted to receiving input signals and providing the input signals to the row and column decoders.

57. (Amended) A flat panel display, comprising:

a field emitter array formed on a glass substrate, wherein the field emitter array includes:

a number of cathodes in rows along a substrate;

a gate insulator located along the substrate and surrounding the cathodes, the gate insulator having a gate line region thickness;

a number of gate lines coupled to the gate insulator, wherein a gate line to cathode distance between a portion of the gate line and the cathode is substantially